1. A method to form a programmable resistor device in an integrated circuit device comprising:

forming a semiconductor layer overlying a substrate;

patterning said semiconductor layer to form a plurality of lines wherein said lines are electrically parallel between a first terminal and a second terminal and wherein any of said lines may be blown open by a current forced from said first terminal to said second terminal; and

selectively forming a metal-semiconductor alloy overlying a first group of said lines but not overlying a second group of said lines.

2. The method according to Claim 1 wherein said semiconductor layer comprises silicon.

3. The method according to Claim 1 wherein said semiconductor layer comprises polysilicon.

4. The method according to Claim 1 wherein said programmable resistor device is a chip identifier for said integrated circuit device.

5. The method according to Claim 1 wherein said metal-

semiconductor alloy comprises metal silicide.

6. The method according to Claim 1 wherein said step of selectively forming a metal-semiconductor alloy comprises:

forming a masking layer overlying said plurality of lines wherein said masking layer covers said second group of lines but exposes said first group of lines;

depositing a metal layer overlying said masking layer and said plurality of lines wherein said metal layer contacts said first group of lines;

annealing said metal layer to form said metal semiconductor alloy overlying said first group of lines; and

removing unreacted said metal layer.

7. The method according to Claim 1 further comprising selectively doping said plurality of lines prior to said step of selectively forming a metal-semiconductor alloy.

8. The method according to Claim 5 wherein said first group of lines is doped and said second group of lines is not doped.

9. The method according to Claim 1 wherein said first group

comprises a single line, wherein said second group comprises more than one line, and wherein said single line comprises a smallest resistance of all of said lines.

10. A programmable resistor device in an integrated circuit device comprising:

a plurality of lines comprising a semiconductor layer overlying a substrate wherein said lines are electrically parallel between a first terminal and a second terminal and wherein any of said lines may be blown open by a current forced from said first terminal to said second terminal; and

a metal-semiconductor alloy overlying a first group of said lines but not overlying a second group of said lines.

11. The device according to Claim 10 wherein said semiconductor layer comprises silicon.

12. The device according to Claim 10 wherein said semiconductor layer comprises polysilicon.

13. The device according to Claim 10 wherein said programmable resistor device is a chip identifier for said integrated circuit device.

14. The device according to Claim 10 wherein said metal-semiconductor alloy comprises metal silicide.

15.The device according to Claim 10 wherein said plurality of lines is doped.

16. The device according to Claim 10 wherein said first group of lines is doped and said second group of lines is not doped.

17. The device according to Claim 10 wherein said first group comprises a single line, wherein said second group comprises more than one line, and wherein said single line comprises a smallest resistance of all of said lines.

18. A method to program a programmable resistor device wherein said device comprises:

a plurality of lines comprising a semiconductor layer overlying a substrate wherein said lines are electrically parallel between a first terminal and a second terminal and wherein any of said lines may be blown open by a current forced from said first terminal to said second terminal; and

a metal-semiconductor alloy overlying a first group of said lines but not overlying a second group of said lines wherein said device comprises a first resistance between said first and second terminals; and wherein said method comprises:

forcing a programming current from said first terminal to said second terminal wherein said programming current causes a first line in said first group to blow such that said device comprises a second resistance between said first and second terminals; and

removing said programming current.

19. The method according to Claim 18 wherein said semiconductor layer comprises silicon.

20. The method according to Claim 18 wherein said programmable resistor device is a chip identifier for said integrated circuit device.

21. The method according to Claim 18 wherein said metal-semiconductor alloy comprises metal silicide.

22. The method according to Claim 18 wherein said plurality of lines is doped.

23.The method according to Claim 22 wherein said first group of lines is doped and said second group of lines is not doped.

24. The method according to Claim 18 wherein said first group comprises a single line, wherein said second group comprises more than one line, and wherein said single line comprises a smallest resistance of all of said lines.

25. The method according to Claim 18 further comprising:

forcing a second programming current from said first terminal to said second terminal wherein said second programming current causes one of said lines in said second group to blow such that said device comprises a third resistance between said first and second terminals; and

removing said second programming current.